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<b>Substitute for form 1449A/PATENT &amp; TRADEMARK OFFICE</b>  <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (use as many sheets as necessary)				<b>Complete if Known</b>	
				Application Number	10/808,895
				Filing Date	March 24, 2003
				First Named Inventor	John R. HUMPHREY et al.
				Group Art Unit	2186
				Examiner Name	Unassigned
Sheet	1	of	1	Attorney Docket Number	10354*3

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. <sup>1</sup>	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code <sup>3</sup> (if known)			

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>4</sup>
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<sup>1</sup> Applicant's unique citation designation number (optional). <sup>2</sup> See attached Kinds Codes of USPTO Patent Documents at [www.uspto.gov](http://www.uspto.gov) or MPEP 901.04. <sup>3</sup> Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). <sup>4</sup> For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the application number of the patent document. <sup>5</sup> Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. <sup>6</sup> Applicant is to place a check mark here if English language Translation is attached.

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, page(s), volume-issue number(s), publisher, city and/or country where published.	
GP		J.R. Marek, "An Investigation of a Design for a Finite-Difference Time Domain (FDTD) Hardware Accelerator," Air Force Institute of Technology, Wright-Patterson AFB, M.S. Thesis (1991).	
↓		J.R. Marek et al., "A Dedicated VLSI Architecture for Finite-Difference Time Domain Calculations," presented at the 8th Annual Review of Progress in Applied Computational Electromagnetics, Naval Postgraduate School, Monterey, California pp. 546-553 (1992).	
↓		R.N. Schneider et al., "Application of FPGA Technology to Accelerate the Finite-Difference Time-Domain (FDTD) Method," presented at the 10th ACM International Symposium on Field-Programmable Gate Arrays, Monterey, California, pp. 97-105 (2002).	
GP		P. Placidi et al., "A Custom VLSI Architecture for the Solution of FDTD Equations," <i>IEICE Trans. Electron.</i> , vol. E85-C, No. 3, pp. 572-577 (March 2002).	

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Attorney Docket No. 10354\*3